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10/670,975	09/25/2003	Kum Foo Leong	884.951US1	8112

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EXAMINER

RODGERS, COLLEEN E

ART UNIT PAPER NUMBER

2813

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 September 2006 has been entered.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4 and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by **Kailasam** (US Patent Application Publication 2005/0181598).

Regarding claim 1, **Kailasam** discloses a method for forming a via in an integrated circuit packaging substrate comprising:

making a via opening 8 (called “feature”) having a base [see Fig. 1], the base of the via opening positioned at a selected level that includes a first conductive material within the integrated circuit packaging substrate [see Fig. 1];

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depositing an interfacial layer material 22 (called “adhesion layer”) within at the base of the opening [see Fig. 2];

placing a second conductive material 24 (called “diffusion barrier”) over the interfacial material 22; and

directing energy to the base of the opening to heat the materials at the base of the opening [see paragraph 0014].

Regarding claim 4, **Kailasam** discloses the method of claim 1 as described above, wherein the interfacial material is a material that will diffuse into at least one of the first conductive material or the second conductive material at the temperature produced by heating the materials at the base of the via opening [see paragraph 0014].

Regarding claim 11, **Kailasam** discloses the method of claim 1 as described above, wherein placing the second conductive material over the interfacial material includes plating copper 32, 34 within the via opening [see paragraph 0014].

Regarding claim 12, **Kailasam** discloses the method of claim 1 as described above, wherein placing the second conductive material over the interfacial material further comprises plating copper by either electroless or electrolytic methods [see paragraph 0014].

Regarding claim 13, **Kailasam** discloses the method of claim 1 as described above, further comprising capping the via 30 [see Fig. 3].

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the

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subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kailasam** (US Patent Application Publication 2005/0181598) in view of **Cohen et al** (US Patent Application Publication 2005/0215046).

Regarding claim 2, **Kailasam** discloses the method of claim 1 as described above. **Kailasam** does not disclose the step of masking the surface of the integrated circuit packaging substrate, a mask being formed having a mask opening therein positioned above to the base of the via opening. **Cohen et al** discloses the use of a conformable contact (CC) mask for use in selective deposition, wherein the conformable material for each mask is shaped in accordance with a cross-section of the material to be plated [see paragraph 0020]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the mask of **Cohen et al** during the deposition steps of **Kailasam** because the conformable material of the CC mask of **Cohen et al** acts as a barrier to electrodeposition [see paragraph 0022].

Regarding claim 3, the prior art of **Kailasam** and **Cohen et al** discloses the method of claim 2 as described above. **Cohen et al** further discloses the step of removing the mask [see paragraph 0023].

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kailasam** (US Patent Application Publication 2005/0181598) in view of **Chan et al** (USPN 6,495,200).

**Kailasam** discloses the method of claim 1 as described above. **Kailasam** does not disclose that the interfacial material may be selected from the group consisting of palladium, platinum, cobalt or nickel. **Chan et al** discloses a method of forming a via including depositing an interfacial layer 13

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within at the base of the opening [see Fig. 1A] and placing a conductive material 16 over the interfacial material 13. Furthermore, **Chan et al** discloses wherein the interfacial material includes palladium [see col. 4, lines 27-34]. It would have been obvious to one of ordinary skill at the time of invention to use palladium as the interfacial material because the application process of dip coating or spin-on is less expensive than the CVD process required to deposit other materials [see col. 4, lines 11-14].

*Allowable Subject Matter*

7. Claims 7-10, 21-27, 31-33 and 35-40 are allowed for reasons deemed to be of record.

*Response to Arguments*

8. Applicant's arguments filed 21 September 2006 have been fully considered but they are not persuasive. With respect to the rejection under 35 U.S.C. §102(e) of claims 1, 4 and 11-13 as anticipated by **Kailasam**, Applicants argue that **Kailasam** fails to anticipate independent claim 1 because **Kailasam** "... is directed at adhering a plateable barrier/seed layer to the dielectric material ... not for connecting a first conductive material to a second conductive material" [see Remarks, page 8]. The Examiner respectfully disagrees. **Kailasam** teaches a heating step that causes "a reaction between the dielectric material, the adhesion layer [first conductive material 22], and the diffusion barrier [second conductive material 24]" [see paragraph 0014].

Furthermore, with respect to claim 1, Applicants argue that **Kailasam** teaches "a general heat treatment not directed toward a base of the opening" [see Remarks, page 9]. The Examiner concedes that the wafer of **Kailasam** is subjected to a general heat treatment; however, the Examiner disagrees that the claim language of the instant independent claim has sufficient specificity

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to be patentably distinct from the heating step of **Kailasam**. By placing the wafer in the oven, heat is directed to the entire wafer (as admitted to by Applicants: "There is no directing of energy other than to the entire wafer" [see Remarks, page 9]), which includes the base of the via.

With respect to the rejection under 35 U.S.C. §103(a) of claims 2 and 3 as unpatentable over **Kailasam** in view of **Cohen et al**, Applicants argue that claims 2 and 3 depend from claim 1, and that **Cohen et al** fail to remedy the alleged deficiencies of **Kailasam**. The Examiner considers **Kailasam** to anticipate claim 1 as explained above; therefore, claims 2 and 3 remain rejected.

With respect to the rejection under 35 U.S.C. §103(a) of claims 5 and 6 as unpatentable over **Kailasam** in view of **Chan et al**, Applicants argue that claims 5 and 6 depend from claim 1, and that **Chan et al** fail to remedy the alleged deficiencies of **Kailasam**. The Examiner considers **Kailasam** to anticipate claim 1 as explained above; therefore, claims 5 and 6 remain rejected.

### *Conclusion*

9. All claims are drawn to the same invention claimed in the earlier application and have been finally rejected on the grounds and art of record in the next Office action when entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

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calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen E. Rodgers whose telephone number is (571) 272-8603. The examiner can normally be reached on Monday through Friday, 9:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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